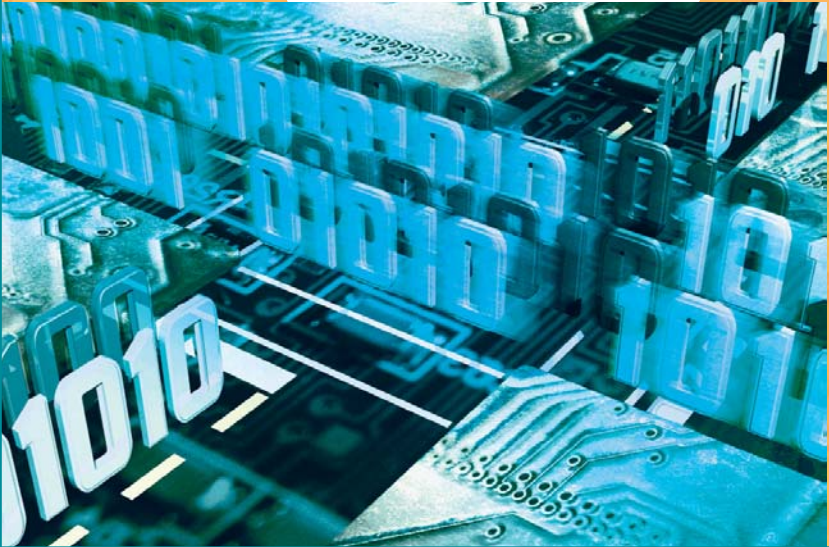




WAVECREST

Understanding the PCI Express™ 1.1 Specification



Quick Guide

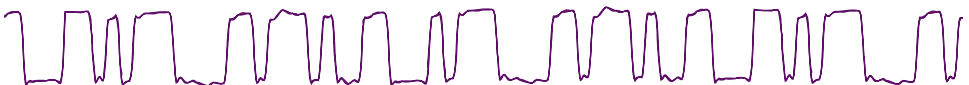
Overview

PCI Express™ represents a major advance in the PC input/output bus architecture. The 66 Mb/s data rate of the PCI bus compared to the current 2.5 Gb/s data rate of PCI Express architecture represents a 38 times increase in speed. In addition, PCI Express architecture allows up to 32 lanes with each running at 2.5 Gb/s, representing an 80 Gb/s data delivery capability for each sub-module system. There are many such sub-modules in a PC system supporting various applications. The physical layer performance of PCI Express is at 10^{-12} bit error rate (BER) for each lane.

Aside from the unprecedented data rate and BER performance goals for PCI Express, the cost requirements are equally challenging. These include:

- ◆ Same or lower cost compared with PCI at the system level.
- ◆ Same or lower cost components (i.e., oscillator or clock generator) and materials (i.e. FR-4 PCBs).
- ◆ Lower cost mainstream CMOS process technology.

The implication of using lower cost components from a signal integrity perspective is that lower cost components are generally noisy or jittery, making the BER of 10^{-12} hard to achieve. Therefore, there needs to be new and innovative designs in order to achieve the same or better performance with the same components.



Why were changes needed to the PCI Express 1.0a Specification and what are the benefits?

The PCI Express 1.0a Specification was based on the technology and knowledge available at the time it was written. In the past two years, as the PCI Express architecture moved from the design phase to characterization, and even to the volume production phase, and as better simulation, modeling, and detailed characterization data became available, it became clear that some aspects of the 1.0a specification were no longer valid or accurate enough to ensure the high performance/low cost production of PCI Express components and systems. Therefore, a more comprehensive and accurate specification was called for.

For example, the jitter specification in the 1.0a document uses the "250/3500" UI testing method. This method was mostly inherited from the USB testing method and was found not to be appropriate and accurate enough to test PCI Express jitter. The "250/3500" UI method implies a 3rd order high-pass jitter transfer function, while the PCI Express data and clock recovery circuit has a 1st order high-pass function. This is off by 2 orders, and results in significant errors during the jitter testing.

It is well known that inaccuracy in testing will result in yield loss. For a commodity product like PCI Express, the volume can be in the order of billions. Even a four decimal yield of 99.999% will result in 10,000 parts scrapped out of a billion; a huge economical loss.



What is the PCI Express 1.1 Specification?

The PCI Express 1.1 jitter specification was developed to achieve the following objectives:

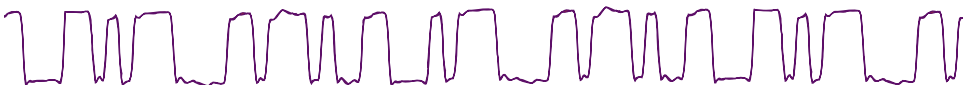
- ◆ Enable better accuracy.
- ◆ Enable better testing methods and test coverage.
- ◆ Provide scalability.
- ◆ Enable jitter budget optimization and ensure interoperability with lower cost.

References at the end of this document give more detailed background information. ^{[1][2]}

Highlights of the major changes from 1.0a to 1.1

The changes to the PCI Express 1.1 jitter specification involves two related specifications. ^{[3][4]}

- ◆ "PCI Express Base Specification 1.1" deals with transmitter, medium, and receiver jitter testing.
- ◆ "PCI Express Card Electromechanical Specification 1.1" deals with reference clock jitter.



Changes for "PCI Express Base Specification 1.1"

- ◆ The clock recovery function of the Rx is defined as a first order high-pass filter with a 3dB bandwidth frequency of 1.5 MHz.
- ◆ The Tx and Rx eye measurements are to be clarified as measurements with a "clean" reference clock (no SSC and no jitter).
- ◆ The Tx eye opening measurement requirement changes from 0.7 UI to 0.75 UI.
- ◆ The Tx PLL 3dB bandwidth frequency must be between 1.5 and 22 MHz, with less than 3dB of peaking in magnitude.
- ◆ The median jitter is specified over a 10^6 sample size using the compliance pattern and the 1st order high-pass filter.

Changes for "PCI Express Card Electromechanical Specification 1.1"

- ◆ Cycle-to-cycle jitter is found to be insufficient to bound the 100 MHz reference clock and a phase jitter (or accumulated jitter) specification is required.
- ◆ 100 MHz reference clock jitter is tested based on its phase jitter and by applying a band-pass jitter transfer function defined in references [3][4].
- ◆ Total jitter (TJ) will be tested to a BER 10^{-12} , or BER 10^{-6} with the assumption of a minimum RJ sigma value.

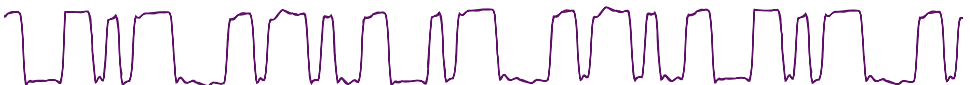


Benefits of the 1.1 Specification

- ◆ Better testing accuracy, high yielding, and high quality.
- ◆ Larger jitter testing solution space: enabling test cost reduction.
- ◆ Scalability: enabling easy future upgrading rather than replacing.
- ◆ Optimized jitter budgets: enabling low-cost system integration with a high interoperability quality.

Wavecrest's Involvement in the PCI Express 1.1 Specification

Wavecrest realized and illustrated the shortfalls of using the "250/3500 UI" method to test PCI Express jitter as defined in the 1.0a specification and brought this to the attention of PCI-SIG electrical working group (EWG) members. As a result, the Jitter Working Group (JWG) was founded with a mission of developing an accurate and complete jitter specification that would meet both performance and cost goals for PCI Express. Wavecrest was an original founding member, along with a few others including top semiconductor companies. Wavecrest Co-Chaired the JWG activities, played a leading role in, and made major contributions to the formation of 1.1 Jitter Specification.



Wavecrest Solutions for testing to the PCI Express 1.1 Specification

Complete solutions for testing to the PCI Express 1.1 Specification are now available from Wavecrest. These solutions include diagnostic and compliance tests for both jitter and signal integrity for design, characterization and high volume production environments.

These solutions were developed from our solid expertise in PCI Express jitter testing, as well as our well-established experience and reputation in dealing with jitter and signal integrity analysis within other serial communication applications, such as SATA, Fibre Channel, and Gigabit Ethernet.

Our solutions extend beyond conventional product offerings as we also provide test method consultation, training and education by working one on one with you and your staff.

References

[1] Li, Martwick, Talbot, Wilstrup, 2004, ITC paper on PCI Express Jitter, ITC Proceedings.

[2] PCI Express Jitter white paper, 2004:
http://www.pcisig.com/specifications/pciexpress/technical_library#jitter

[3] PCI Express 1.1 spec, review draft, 2004:
http://www.pcisig.com/specifications/pciexpress/review_zone#express

[4] PCI Express jitter ECN, 2004:
http://www.pcisig.com/specifications/pciexpress/review_zone#jitter





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